REMARKS/ARGUMENTS

Claims 1-16 are pending in this application and claims 17-19 are added by this response. Claims 12 and 16 are amended to correct typographical errors in the claims as noted in the Office Action. Claims 1-8 are amended to omit reference to a "first" request as there is only one request called for in the claims and therefore "first" is not necessary. Claim 9 is amended to provide clearer antecedent basis for claims 12, 13 and 15. Claims 14 and 16 are amended to clarify the language. These amendments are not intended to further limit the claims or to add new elements to the claims, unless specifically argued below.

Independent claims 1 and 9 are also amended to clarify that the claims relate to systems in which modules other than a processing unit are enabled to initiate cache coherency transactions over a system bus. These amendments are believed to more distinctly describe the subject matter of the invention and better distinguish over the relied on references.

A. Specification

The specification is amended to correct informalities in the specification as filed. No new matter is added by these amendments.

B. Claim Objections

The amendments to claims 12 and 16 are believed to overcome the objections raised in the Office action.

C. Rejections under 35 U.S.C. 112

Claims 12-14 and 16 were rejected under 35 USC 112 as indefinite. This rejection is respectfully traversed. The amendments to claims 9 and 12 provide clearer antecedent basis for the term "state of the cache memory" as well as to

provide clearer support for "the cache" as that term appears in claim 13. Although not noted in the Office Action, claims 15 and 16 also included the term "the cache", hence, the amendment to claim 9 places claims 15 and 16 in better form as well. Further, claims 14 and 16 are amended to improve correspondence with the language of independent claim 9 from which they depend. Accordingly, it is requested that the rejections under 35 U.S.C. 112 be withdrawn.

D. Rejections under 35 U.S.C. 102

Claims 1-4 and 9-12 were rejected under 35 USC 102 as being anticipated by Arimilli et al (US Patent No. 6,418,514). The rejection is respectfully traversed.

It should be noted that the previously presented amendment offering to limit the claims to a single processor system has been withdrawn by this amendment. This limitation was not necessary to distinguish over the relied on references. It has become known that multiple processors are an equivalent to single processors. The present invention includes systems in which the processor component is implemented as multiple processors. In other words, of the plurality of modules, more than one module may be considered a "processor". By removing the single processor limitation of claims 1 and 9 it is explicitly intended that the claim scope include the equivalent structures.

Independent claim 1 calls for, amongst other limitations, a computer system in which one of a plurality of system components other than the processor is able to request a cache coherency operation. Further, claim 1 calls for the cache coherency operation to be performed by the processor in response to the request. The Arimilli et al. do not show or suggest this feature of claim 1.

First, the transaction-based bus of claim 1 is not fairly shown or suggested by a cache operations queue as taught in Arimilli et al. A "bus" commonly refers to one or more signal lines or conductors that connect devices within a system. The

instant specification describes a transaction based bus on page 7 as a bus that implements a transaction set, where each transaction comprises a request/response pair. In contrast, a queue is well known to be a list or stack. Arimilli et al. teach that the queue is coupled to a bus, but the queue is not itself a bus. It is respectfully believed that referring a queue as a bus mischaracterizes the reference. Moreover, the stated reasoning for calling a queue a bus is that "the operations queue contains a serialized list of cache operations..." However, the transaction-based bus of claim 1 does not "contain a serialized list". Accordingly, by the same logic used in the Office action, Arimilli's queue 68(a) is not the same as the transaction-based bus of claim 1.

Arimilli et al. do, however, show a bus 54 that is coupled to cache 56a. However, bus 54 is not directly coupled to a processor as called for in claim 1. Hence, the processor cannot respond to a request from a system component other than the processor by performing a cache coherency operation. To further clarify this distinction, claim 1 is amended to specify that the system components other than the processor access main memory directly through the transaction based bus mechanism, but do not access the cache memory directly. Arimilli et al. teach only a system in which the cache memory 56 is coupled directly to the system bus 54.

For at least these reasons, claim 1 is not anticipated by Arimilli et al. Claims 2-4 that depend from claim 1 are allowable for at least the same reasons as claim 1.

Claim 9 calls for, among other things, initiating a cache coherency transaction on the system bus using one of the plurality of modules other than the processing unit; and causing the processing unit to execute a cache coherency operation. It is believed that the Office Action fails to state a prima facie case of obviousness with respect to the method steps of claim 9. One cannot discern from the office action what activity in Arimilli et al. is being relied on to show the step of

initiating a cache coherency transaction on the system bus, or what causes the processing unit to execute a cache coherency transaction. Additional clarification is respectfully requested.

In Arimilli, any cache transaction that is broadcast on system bus 54 is initiated by a cache 56 itself. Hence, Arimilli et al. do not cause the processing unit to execute a cache operation in response to a cache coherency transaction on system bus 54. Because processor bus 66a is clearly separate from system bus 54, it would appear that Arimillie specifically require that cache coherency transactions be handled directly from one cache 56 to another cache 56. Since the queue controller 70 acts as a gate to restrict broadcast of unnecessary coherency operations, the Arimilli et al system would not operate if the coherency operations were implemented by a processor as called for in claim 9.

For at least these reasons claim 9 and claims 10-12 that depend from claim 9 are neither anticipated nor made obvious by the relied on references.

E. Rejections under 35 U.S.C. § 103

Claims 5, 6, 13, and 14 stand rejected under 35 USC 103(a) as being unpatentable over Arimilli et al and Spencer (US Patent No. 6,295,582). This rejection is respectfully traversed.

Claims 5 and 6 distinguish over Arimilli et al. for at least the same reasons as claim 1 from which they depend. Claims 13 and 14 distinguish over Arimilli et al. for at least the same reasons as claim 9 from which they depend. Spencer does not supply the deficiencies of Arimilli set out above. Moreover, with respect to claims 5 and 13, Spencer does not show or suggest a cache flush operation that is conducted over a transaction-based bus such as memory bus 108 or PCI bus 110. Claims 5 and 13 do not simply define a cache flush transaction, but also define that the cache flush transaction is *the* cache coherency transaction defined within the

transaction set of the transaction based bus mechanism. Spencer performs a cache flush operation, but does not show or suggest a cache flush transaction. With respect to claims 6 and 14, Spencer does not show or suggest a response addressed to the system component that generated the request.

Claims 7, 8, 15, and 16 stand rejected as being unpatentable over Arimilli et al and Jacobs (US Patent No. 6,047,358). This rejection is respectfully traversed.

Jacobs does not supply the deficiencies of Arimilli et al. set out above. Moreover, with respect to claims 7 and 15, Jacobs does not show or suggest a cache purge operation that is conducted over a transaction-based bus. Claims 7 and 15 do not simply define a cache purge operation, but also define that the cache flush transaction is *the* cache coherency transaction defined within the transaction set of the transaction based bus mechanism. In the case of claims 8 and 16, Jacob does not show or suggest a response addressed to the system component that generated the request.

In view of the above, it is respectfully believed that claims 5-8 and 13-16 are not shown or suggested by the combined references and that the rejection should be withdrawn.

F. New claims 17, 18 and 19.

Newly presented claims 17 and 18 are believed to be allowable because the relied on references fail to show or suggest a computing device in which a processor and various system components are coupled to a transaction-based bus that defines a cache transaction even though the cache memory is not coupled directly to the transaction-based bus. The references taken for all that they teach suggest, at most, defining cache operations on a bus/interconnect only when a cache memory is coupled to that bus/interconnect. For at least these reasons claims 17 and 18 are believed to be allowable.

Claim 19 depends from claim 1 and further specifies several specific types of system components other than the processor that may be used to issue requests indicating a request to perform a cache coherency operation. The relied on references do not show or suggest such devices being enabled to issue requests indicating a request to perform a cache coherency operation.

G. Conclusion

In view of all of the above, claims 1-16 are believed to be allowable over the cited references and the case in condition for allowance which action is respectfully requested. Should the Examiner be of the opinion that a telephone conference would expedite the prosecution of this case, the Examiner is requested to contact Applicants' attorney at the telephone number listed below.

No fee is believed due for this submittal. However, any fee deficiency associated with this submittal may be charged to Deposit Account No. 50-1123.

Respectfully submitted,

1/8, 2004

Stuart T. Langley, No. 33,940
Hogan & Hartson LLP
One Tabor Center
1200 17th Street, Suite 1500
Denver, Colorado 80202
(720) 406-5335 Tel
(303) 899-7333 Fax